

What is claimed is:

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1 1. An apparatus comprising:  
2 a memory device having a memory device input data bus including a least  
3 significant bit and a plurality of non-least significant bits; and  
4 a first repair router having a first repair router input data bus including a least  
5 significant bit and a plurality of non-least significant bits, and a first repair router  
6 output data bus coupled to the memory device input data bus, the first repair router  
7 having internal routing circuitry to route any of the plurality of non-least significant  
8 bits of the first repair router input data bus to the least significant bit of the memory  
9 device input data bus.

1 2. The apparatus of claim 1 wherein:  
2 the plurality of non-least significant bits includes a next-to-least significant  
3 bit; and  
4 the first repair router further includes additional repair routing circuitry to  
5 route any of the non-least significant bits to the next-to-least significant bit.

1 3. The apparatus of claim 1 wherein the memory device includes a memory  
2 device output data bus including a least significant bit and a plurality of non-least  
3 significant bits, the apparatus further comprising:  
4 a second repair router having a second repair router input data bus coupled to  
5 the memory device output data bus, and having a second repair router output data bus  
6 including a least significant bit and a plurality of non-least significant bits, the  
7 second repair router having internal routing circuitry to route the least significant bit  
8 of the memory device output data bus to any of the plurality of non-least significant  
9 bits of the second repair router output data bus.

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1 4. The apparatus of claim 3 wherein the memory device includes a plurality of  
2 address ranges, and the first and second repair routers include address decoding  
3 circuitry to decode each of the plurality of address ranges.

1 5. The apparatus of claim 4 wherein the memory device includes two address  
2 ranges defined by a state of a most significant address bit.

1 6. The apparatus of claim 3 further comprising a display device coupled to the  
2 second repair router output data bus.

1 7. The apparatus of claim 6 wherein the display device is a color display device,  
2 and the memory device and first and second repair routers influence a first color of  
3 the color display device, the apparatus further comprising:  
4 a second memory device; and  
5 a second pair of repair routers coupled to the second memory device to  
6 influence a second color of the color liquid crystal display.

1 8. The apparatus of claim 7 further comprising:  
2 a third memory device; and  
3 a third pair of repair routers coupled to the third memory device to influence  
4 a third color of the color liquid crystal display.

1 9. A memory device comprising:  
2 a plurality of addressable memory locations, each including a least significant  
3 bit and a plurality of non-least significant bits; and  
4 a first repair router having a repair router input data bus with a least  
5 significant bit and a plurality of non-least significant bits, and having a repair router  
6 output data bus coupled to the plurality of addressable memory locations, the first  
7 repair router including routing circuitry to route any of the plurality of non-least

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8 significant bits of the repair router input data bus to the least significant bit of at least  
9 one of the plurality of addressable memory locations.

1 10. The memory device of claim 9 wherein:  
2 the plurality of addressable memory locations are arranged into a plurality of  
3 address ranges; and  
4 the first repair router further includes address decoding circuitry to decode  
5 each of the plurality of address ranges.

1 11. The memory device of claim 10 further comprising a second repair router  
2 coupled to an output data bus of the memory device, the second repair router  
3 including routing circuitry to reverse any routing performed by the first repair router.

1 12. The memory device of claim 9 wherein the first repair router is configured to  
2 route a specific non-least significant bit to the least significant bit of the plurality of  
3 addressable memory locations when a problem exists with the specific non-least  
4 significant bit in at least one of the plurality of addressable memory locations.

1 13. The memory device of claim 9 further comprising a second repair router  
2 coupled to an output data bus of the memory device, the second repair router  
3 including routing circuitry to reverse any routing performed by the first repair router.

1 14. The memory device of claim 9 wherein:  
2 the plurality of non-least significant bits includes a next-to-least significant  
3 bit; and  
4 the first repair router further includes routing circuitry to route any of the  
5 plurality of non-least significant bits of the repair router input data bus to the next-to-  
6 least significant bit of at least one of the plurality of addressable memory locations.

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- 1 15. A display system comprising:  
2 a display device having an array of pixels;  
3 a memory having a plurality of addresses, each of the plurality of addresses  
4 corresponding to one pixel in the array of pixels, and each of the plurality of  
5 addresses including a least significant data bit and a plurality of non-least significant  
6 data bits; and  
7 a repair router to utilize the least significant bit of at least one of the plurality  
8 of addresses to hold non-least significant information.

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- 1 16 The display system of claim 15 wherein the display device is a silicon light  
2 modulator.

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- ~~1 17. The display system of claim 15 wherein the memory is configured to hold a  
2 first color information, the display system further comprising:  
3 a second memory configured to hold second color information; and  
4 a second repair router coupled to the second memory.~~

- 1 18. The display system of claim 17 further comprising:  
2 a third memory configured to hold third color information; and  
3 a third repair router coupled to the third memory.

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- 1 20. An integrated circuit comprising:  
2 a memory device having an input data bus and an output data bus; and  
3 first and second repair routers coupled to the input data bus and the output  
4 data bus, respectively, the first and second repair routers including routing circuitry

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5 to route data to and from the memory device as a function of defects in the memory  
6 device.

1 21. The integrated circuit of claim 20 further comprising a reflective electrode  
2 coupled to the memory, the reflective electrode having a plurality of pixels  
3 responsive to data from the memory device as received by the second repair router.

1 22. The integrated circuit of claim 21 wherein:  
2 the memory device includes a plurality of groups of data locations; and  
3 the first and second repair routers each include circuitry to separately route  
4 data for each of the plurality of groups of data locations.

1 23. The integrated circuit of claim 22 further comprising:  
2 second and third memory devices; and  
3 second and third pairs of repair routers coupled to the second and third  
4 memory devices respectively.